WIDEBAND AGILE TRANSVERSAL FILTER

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Abstract

The development of a Wideband Agile Transversal Filter is made possible by the use of dual gate GaAs FET transistor arrays.

The transversal filter design has a bandwidth of greater than 2.0 GHz and the filter transfer function can be changed in less than 10 nanoseconds. The design has been configured in a four seciton block that can be cascaded to obtain multiple delay functions and thus very complex filter transfer functions.

Introduction

Multisection wideband agile transversal filters are useful for certain types of receivers, signal equalization and matched filter design. This work was undertaken to demonstrate the performance that can be achieved using dual-gate, GaAs MESFET arrays as the active element in transversal filters.

The dual-gate GaAs FET arrays provide the small size, wide bandwidth and very high input impedance necessary for the transversal filter. The functional diagram of the four section transveral filter (Figure 1) shows the filter has been configured to be cascadable to obtain a large number of taps. The four section filter contains two dual-gate GaAs FET arrays mounted on a 2" x 1" ceramic substrate, also containing the 0.5 nanosecond tap delays.

The performance data of the four section unit shows that a useful bandwidth of 2.0 GHz can be obtained using this relatively simple design approach. Performance at the 2.4 GHz band edge can be improved by better control of the transmission line impedance. The filter transfer function can be changed in less than 10 nanoseconds.

Transversal Filter Function

The four stage element, shown in Figure 1, can be shown to have a relatively simple filter characteristic given by:

$$\left|H(f)\right|^2 = \left|\sum_{n=1}^{4} a_n e^{-j2\pi(n-1)f\tau}\right|^2$$

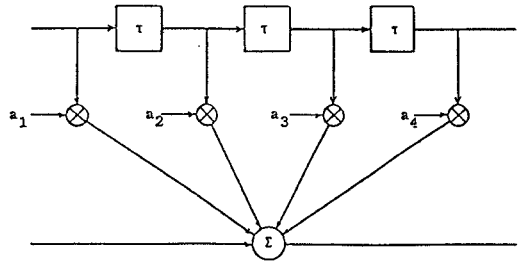

Figure 1: Four Stage Variable Transversal Filter

An example of a possible filter function is shown in Figure 2.

In many situations, however, substantially longer filter structures may be required. This need can be accommodated by cascading these four section elements. Further, the use of non-uniform tap spacing may provide a savings in hardware complexity without loss in performance.

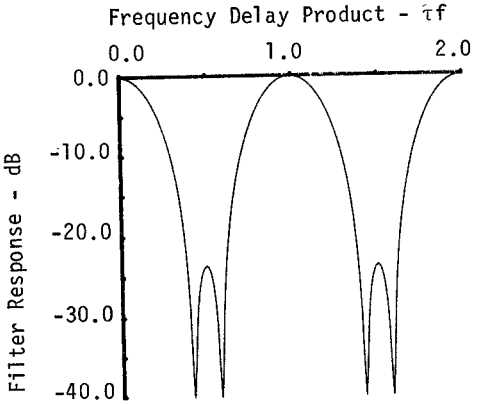

Figure 2: Ideal Filter Response with Tap Weights (1,1.752,1)

Circuit Requirements

Dual-gate MESFET's are used as the active element performing the weighting function in the transversal filter. A dual-gate transistor can be effectively modeled as two single-gate transistors connected in cascode. With the lower transistor biased as a voltage variable resistor the drain current is given by:

$$I_D = \beta V_{DS2}[2(V_{GS2}-V_P)-V_{DS2}]$$

where β is indicative of the transistor tranconductance and V_P is pinch-off voltage. The small signal drain-to-source conductance, defined as:

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}}$$

is given by :

$$g_{ds2} = 2\beta[V_{GS2}-(V_{DS2}+V_P)]$$

which is a linear function of V_{GS2}.

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The dual-gate MESFET can then be considered to be a common-source amplifier with a variable source resistance. This circuit has a gain characteristic given approximately by:

$$A_V = - \frac{R_L}{R_S}$$

where R_L is the load resistance and R_s is the source resistance. The dual-gate MESFET then has a gain characteristic given by:

$$A_V = -2\beta R_L [V_{GS2} - (V_{DS2} + V_p)]$$

which approximates a two-quadrant multiplier.

In order to obtain four-quadrant action, as ideally required in the transversal filter, two two-quadrant circuits are used. One circuit is driven by the signal to be filtered and the other is driven by its complement. This system is shown in Figure 3. The complementary signals can be generated using a balan. The circuit described here has the advantage that any signal feeding through would ideally be cancelled by the feedthrough of the complementary amplifier.

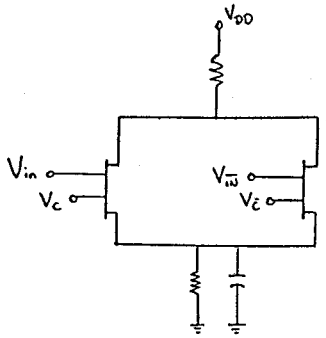

Figure 3: Tap Multiplier Circuit

Further circuit performance characterization was carried out by means of computer simulation. The SPICE 2 JFET model was used to model the GaAs MESFET. This was done because of the ease in obtaining D.C. and A.C. circuit responses. While the limitations of the SPICE JFET model are recognized, the errors introduced by its use are believed to be of the same order of magnitude as the errors due to processing uncertainties.

Of primary interest in the design of the transversal filter is the determination of the input impedances and the output to input isolation. The results of these simulations are shown in Figures 4 and 5, respectively. The data is shown for three values of lower gate voltage corresponding to full on, full off and an intermediate value.

Device Fabrication

The GaAs MESFET array which comprises the heart of the transversal filter is shown in Figure 6. The array contains 4 dual-gate transistors with common sources and drains. The gates are 150 micrometers wide by 1 micrometer in length. The chip dimensions are 25 mils by 25 mils.

The dual-gate GaAs MESFET array were fabricated using standard processing technology. The n-type 800 ohm/sq, active layers were formed by implanting ^{30}Si at 100 keV directly into high

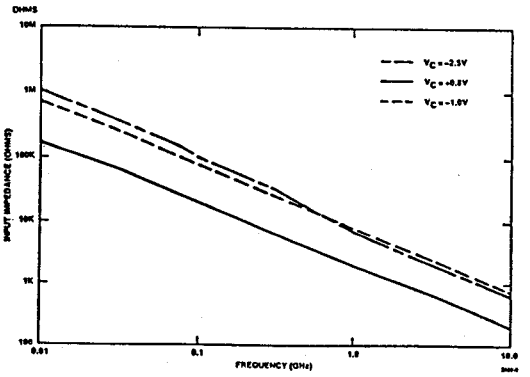

Figure 4: Dual-Gate FET Input Impedance

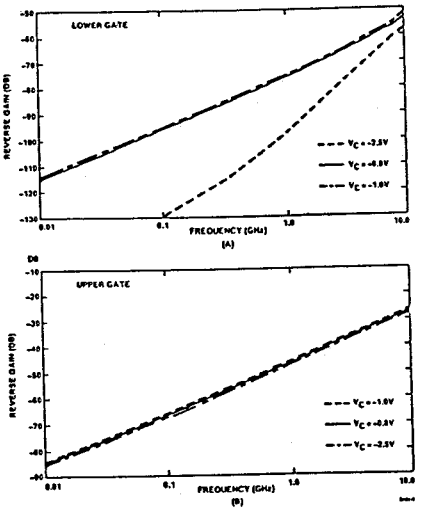

Figure 5: Dual-Gate FET Output to Input Isolation

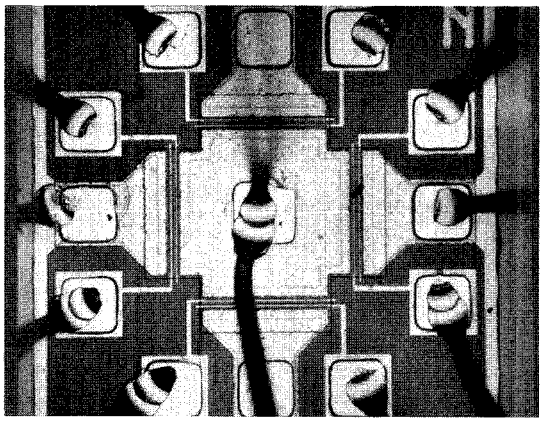

Figure 6: Dual-Gate GaAs MESFET Array

resistivity, chromium doped GaAs substrates. The ion implanted layer was activiated by capping the wafer with silicon nitride and annealing at 850°C for 15 min. Mesa etching was used to achieve device isolation. Source and drain ohmic contacts were formed by alloying evaporated AuGe/Ni at 460°C for 2.5 minutes. The gate and pad metallization were defined using evaporated Ti/Pt/Au and

chlorobenzene assisted lift-off. The 1 micrometer gates are separated by 5 micrometers and centered in a 15 micrometer source-drain spacing. The 0.6 mm x 0.6 mm die is passivated with polyimide. Typical dc characteristics of the 150 micrometer wide, dual-gate MESFETs are V_p = 3.0V, I_{DSS} = 13 ma, and g_m = 8 mS at 50% I_{DSS}.

Circuit Performance

The transversal filter circuitry was constructed on a ceramic substrate using the GaAs transistor array described ealier. Micro-strip transmission lines, with 75 Ω characteristic impedance, were used to form the delay elements. The circuitry is shown in Figure 7.

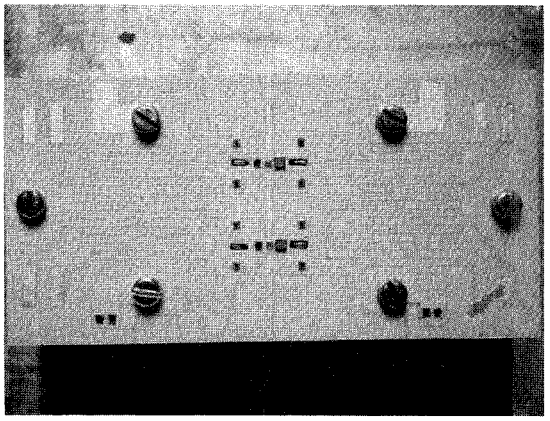

Figure 7: Transversal Filter Hardware

Initially, the impedance characteristics of the delay lines were determined using Time Domain Reflectometry (TDR). Figure 8 shows the TDR results with all gates off and with one gate fully on. The similarity between the two results indicate that the gates only very slightly load the transmission line.

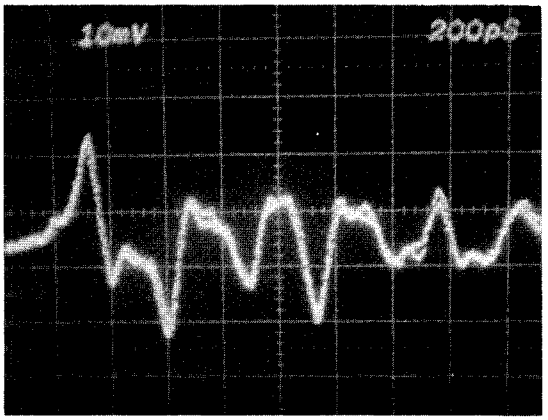

Figure 8: Delay Element TDR (40 mρ/div)

Figures 9 and 10 show the filter pulse responses and frequency responses for various tap settings. The filter rise times are seen to vary from 200 psec for the early taps to 350 psec for the later taps. This effect is primarily due to the low pass characteristics of a long transmission line. The frequency response data indicates the circuit to have a useful bandwidth of 2 GHz. Further, these figures demonstrate the possibility of synthesizing rather sophisticated filter responses.

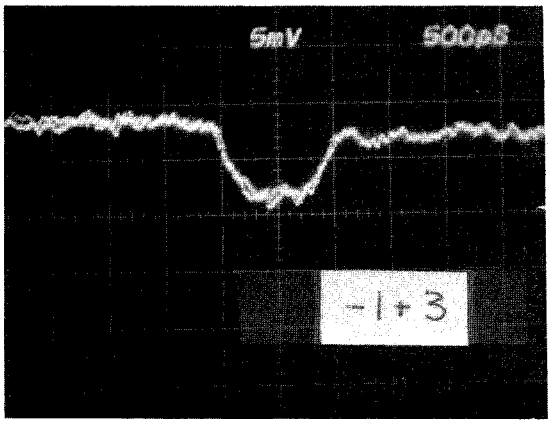

Figure 9: Example Filter Step Responses

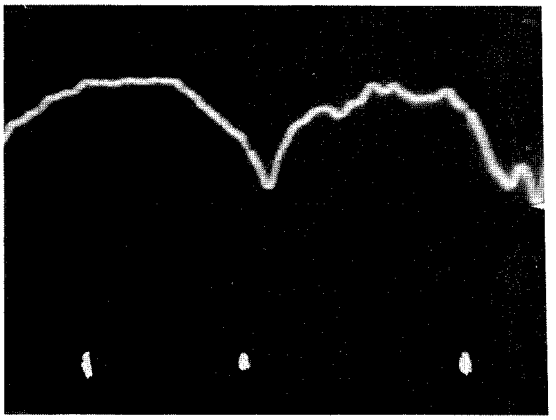

Figure 10: Example Filter Frequency Responses (markers at 0.5,1.0, 2.0 GHz 10dB/div)

Conclusion

Using a relatively simple design a transversal filter has been constructed with a bandwidth of 2 GHz. This filter uses GaAs MESFET dual-gate transistor arrays to weight and sum the delayed samples. The four-section filter constructed here is easily cascadable, thus, making possible construction of very long, sophisticated filters. Finally, since the tap weights can be changed very quickly (<10 nsec) this transversal filter could be an integral part of a high speed adaptive equalization scheme.